



CYPR-CD00055

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of )  
 )  
Merchant, et al. )  
 )  
Serial No. 09/684,160 )  
 )  
Filing Date: October 4, 2000 )  
 )  
For: Method and System for )  
Generating A Bit Order Data )  
Structure Of Configuration Bits )  
From A Schematic Hierarchy )  
 )

Examiner: Hamilton, M.G.

Art Unit: 2172

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OCT 14 2004

Technology Center 2100

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

TERMINAL DISCLAIMER TO OBVIATE

DOUBLE PATENTING REJECTION (37 CFR § 1.321(c))

Dear Sir:

1. Name of Assignee: Cypress Semiconductor Corporation

Address of Assignee: 3901 North First Street, San Jose, CA 95134

2. The Assignee certifies to the best of Assignee's knowledge and belief that Assignee has the entire right, title, and whole interest in and to the above referenced patent application, and represent that the undersigned is authorized to sign on behalf of the above-referenced Assignee.

3. On information and belief, a copy of an Assignment or other documents that evidences placement of title of the above-referenced Application in the Assignee is recorded with the United States Patent and Trademark Office at:

Serial No. 09/684,160  
Terminal Disclaimer

-1-

CYPR-CD00055  
Examiner: Hamilton, M.G.

10/08/2004 SSESHE1 00000007 09684160

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Frame: 0741

Recorded on: October 4, 2000

A certificate under 37 CFR 3.73(b) is attached hereto regarding the above and establishing the right of the assignee to take action in the above referenced patent application.

4. Disclaimer

The terminal part of the statutory term of any patent granted on the above-identified application, which would extend beyond the expiration date of the full statutory term defined in 35 U.S.C. 154 to 156 and 173, as presently shorted by any terminal disclaimer, of the prior United States Patent No. 6,490,712 forming the basis of the double patenting rejection is hereby disclaimed except as provided below, and it is agreed that any patent so granted on the above-identified application shall be enforceable only for, and during, such period that the legal title to said patent shall be the same as the legal title to prior United States Patent No. 6,490,712; this agreement to run with any patent granted on the above-identified application and to be binding upon the grantee, its successors or assigns.

In making the above disclaimer, disclaimant does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term as defined in 35 U.S.C. 154 to 156 and 173 of the prior United States Patent No 6,490,712 in the event that it later: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R.


1.321, has all claims canceled by a reexamination certificate, is reissued in any matter or is terminated prior to expiration of its full statutory term as presently shortened by any terminal disclaimer, except for the separation of legal title stated above.

5. Fee Payment. Enclosed is a check in the amount of \$110.00, under 37 CFR § 1.20(d). The attorney of record is empowered to sign on behalf of Assignee.

6. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: 10/1, 2004

Respectfully submitted,  
WAGNER, MURABITO & HAO, LLP

  
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CERTIFICATE UNDER 37 CFR 3.73(b)

Applicant: Merchant, et al.

Application No.: 09/684,160 Filed: October 4, 2000

For: Method and System for Generating A Bit Order Data Structure Of From A Schematic Hierarchy Configuration Bits

Cypress Semiconductor, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

certify that they are the assignees of the entire right, title and interest in the patent application identified above by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application identified above. The assignment was recorded in the Patent and Trademark office at Reel 011210, Frame 0741, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s) of the patent application identified above, to the current assignee as shown below:

1. From: \_\_\_\_\_ To: \_\_\_\_\_  
The document was recorded in the Patent and Trademark Office at  
Reel \_\_\_\_\_, Frame \_\_\_\_\_, or for which a copy thereof is attached.

2. From: \_\_\_\_\_ To: \_\_\_\_\_  
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☐ Copies of assignments or other documents in the chain of title are attached.

The undersigned has reviewed all the documents in the chain of title of the patent application identified above and, to the best of undersigned's knowledge and belief, title is in the assignees identified above.

The undersigned (whose title is supplied below) is empowered to act on behalf of the assignees.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Name: Ronald M. Pomerence Title: Attorney

Signature: Ronald M. Pomerence Date: 10/1/04